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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,609	10/31/2003	Oz Weisler	100.475US01	9939

7590 06/21/2007

Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339

EXAMINER	
LEE, BETTY E	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
06/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,609	WEISLER ET AL.	
	Examiner	Art Unit	
	Betty Lee	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 19 is objected to because of the following informalities: Claim 19 repeats the limitation "the input memory includes a plurality of banks of memory in which a plurality of input frames are stored by the field programmable gate array" twice. Applicant should remove the second instance.

Appropriate correction is required.

2. Applicant is advised that should claims 4 and 5 be found allowable, claim 5 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **1-8 and 11-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adam et al. (US 6,714,537) in view of Lien et al. (US 6,301,696).

Regarding claim 1, 11, 13, 14, and 15, Adam teaches an input memory and an output memory (see Fig. 4 Boxes 410 and 426); and where an input frame having a plurality of input channels is stored in the input memory (see Fig. 4 Box 410); and where an output frame having a plurality of output channels is stored in the output memory (see Fig. 4 Box 426); where there further includes a map memory in which is stored at least one mapping that specifies one of the plurality of input channels that is mapped to

one of the output channels (see Fig. 5 Box 422). Adam teaches all the subject matter of the claimed invention with the exception of a FPGA. However, Lien teaches implementing a system on a FPGA (see col. 13 lines 36-38). Thus, it would have been obvious to one of ordinary skill in the art to implement this system on a FPGA. The motivation to do so is to allow for flexibility in design changes (see Lien col. 13 lines 36-45).

Regarding claim 2, Adam further teaches that each of the input channels corresponds to a plurality of time slots (see col. 2 lines 41-49; Frames comprise a plurality of time slots.).

Regarding claim 3, Adam further teaches that each of the output channels corresponds to one of a plurality of time slots (see col. 2 lines 41-49; Frames comprise a plurality of time slots.).

Regarding claims 4, 5, 16, and 19, Adam further teaches where the input memory includes a plurality of banks of memory in which a plurality of input frames are stored (see Fig. 4 Boxes 410-D and 410-n). Adam teaches all the subject matter of the claimed invention with the exception of a FPGA. However, Lien teaches implementing a system on a FPGA (see col. 13 lines 36-38). Thus, it would have been obvious to one of ordinary skill in the art to implement this system on a FPGA. The motivation to do so is to allow for flexibility in design changes (see Lien col. 13 lines 36-45).

Regarding claim 6, Adam further teaches a logic block that includes an input interface, where the input interface stores the input frame in the input memory (see Fig. 2 Box 214). Adam teaches all the subject matter of the claimed invention with the

exception of a FPGA. However, Lien teaches implementing a system on a FPGA (see col. 13 lines 36-38). Thus, it would have been obvious to one of ordinary skill in the art to implement this system on a FPGA. The motivation to do so is to allow for flexibility in design changes (see Lien col. 13 lines 36-45).

Regarding claim 7, Adam further teaches a state machine block, where the state machine block reads one of the plurality of input channels of the input frame stored in the input memory and writes the input channel to one of the plurality of output channels of the output frame stored in the output memory (see Fig. 4 Box 418). Adam teaches all the subject matter of the claimed invention with the exception of a FPGA. However, Lien teaches implementing a system on a FPGA (see col. 13 lines 36-38). Thus, it would have been obvious to one of ordinary skill in the art to implement this system on a FPGA. The motivation to do so is to allow for flexibility in design changes (see Lien col. 13 lines 36-45).

Regarding claim 8, Adam further teaches the state machine block reads the mapping from the map memory (see Fig. 4 Boxes 218 and 422).

Regarding claim 12, Adam further teaches means for reading the at least one of the input channels of the input frame from the means for storing the input frame; and means for writing to the means for storing the output frame the at least one of the input channels of the input frame in the corresponding one of the plurality of channels of the output frame (see col. 4 lines 35-49).

Regarding claim 17, Adam further teaches where the system reads one of the plurality of input channels stored in the memory and writes the input channel to on of the

plurality of output channels of the output frame stored in the output memory (see col. 4 lines 35-49). Adam teaches all the subject matter of the claimed invention with the exception of a FPGA. However, Lien teaches implementing a system on a FPGA (see col. 13 lines 36-38). Thus, it would have been obvious to one of ordinary skill in the art to implement this system on a FPGA. The motivation to do so is to allow for flexibility in design changes (see Lien col. 13 lines 36-45).

Regarding claim 18, Adam further teaches that each of the input channels corresponds to a plurality of time slots (see col. 2 lines 41-49; Frames comprise a plurality of time slots.) and each of the output channels corresponds to one of a plurality of time slots (see col. 2 lines 41-49; Frames comprise a plurality of time slots.).

7. Claims **9, 10, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adam et al. (US 6,714,537) as applied to claims 1 and 13 above, and further in view of Ellersick et al. (US 6,038,226).

Regarding claim 9, Adam teaches an input memory (see Fig. 4 Box 410). Adam teaches all the subject matter of the claimed invention with the exception of a dual ported random access memory. However, Ellersick teaches using a dual ported memory in a time slot interchange circuit (see col. 1 line 58 – col. 2 line 2). Thus, it would have been obvious to one of ordinary skill in the art to use the system of Ellersick in the system of Adam. The motivation for doing so is to make the system more efficient.

Regarding claim 10, Adam teaches an output memory (see Fig. 4 Box 426). Adam teaches all the subject matter of the claimed invention with the exception of a dual ported random access memory. However, Ellersick teaches using a dual ported memory in a time slot interchange circuit (see col. 1 line 58 – col. 2 line 2). Thus, it would have been obvious to one of ordinary skill in the art to use the system of Ellersick in the system of Adam. The motivation for doing so is to make the system more efficient.

Regarding claim 20, Adam teaches an input memory (see Fig. 4 Box 410) and an output memory (see Fig. 4 Box 426). Adam teaches all the subject matter of the claimed invention with the exception of a dual ported random access memory. However, Ellersick teaches using a dual ported memory in a time slot interchange circuit (see col. 1 line 58 – col. 2 line 2). Thus, it would have been obvious to one of ordinary skill in the art to use the system of Ellersick in the system of Adam. The motivation for doing so is to make the system more efficient.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wellbaum et al. (US 2003/0189925), Ohtawa (US 5,130,979), and Etemadi et al. (US 2004/0028051) are all cited to show systems which are considered pertinent to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Betty Lee whose telephone number is (571) 270-1412. The examiner can normally be reached on Monday-Thursday 9-5 EST and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BL

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600